IN THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of All Pending Claims

1. - 20. (canceled)

21. (currently amended) A method for reducing effects of spurious frequencies in a wireless communications device, the method comprising:

operating a transceiver in a first mode of operation comprising one of an analog mode and a digital mode;

selecting a first passband frequency range of a plurality of selectable passband frequency ranges, the first passband frequency range corresponding to the first mode of operation;

operating a processor in the first mode of operation at a first processor clock frequency of a plurality of processor clock frequencies;

switching operation of the transceiver to a second mode of operation comprising the <u>other of the</u> analog mode and the digital mode;

selecting a second passband frequency range of the plurality of selectable passband frequency ranges, the second passband frequency range corresponding to the second mode of operation;

operating the transceiver in the second mode of operation using the selected second passband frequency range;

selecting a second processor clock frequency of the plurality of processor clock frequencies that produces no substantial spurious signals in the selected second passband frequency range;

operating the processor at the selected second processor clock frequency; and

maintaining operation of the processor with the selected second processor clock frequency during the operation of the transceiver in the second mode of operation and at the selected second passband frequency range.

22. (previously presented) The method of claim 21, wherein the analog mode is advanced mobile phone service (AMPS); and wherein the digital mode is code division multiple access mode (CDMA).

23. (previously presented) The method of claim 21, wherein the second mode is advanced mobile phone service (AMPS) with the selected second passband frequency range having a center frequency of approximately 900 megahertz (MHz); and

wherein the first mode is the code division multiple access mode (CDMA) utilizing the first processor clock frequency at 19.2 megahertz (MHz) with a 46^{th} harmonic at 883.2 MHz.

24. (previously presented) The method of claim 23, wherein the step of selecting the second processor clock frequency further comprises the step of:

increasing the first processor clock frequency from 19.2 MHz to 26.24 MHz .

25. (previously presented) A method for reducing effects of clock harmonics in a wireless communications device, the method comprising:

selecting a first operation mode;

generating a first transceiver carrier frequency for the passband of the first operation mode;

generating a first clock frequency for operating at least one circuit of the wireless communications device as long as the first operation mode is selected, the first clock frequency having a plurality of first harmonic frequencies;

selecting a second operation mode;

generating a second transceiver carrier frequency for the passband of the second operation mode;

changing the first clock frequency to a second clock frequency with a plurality of second harmonic frequencies so that none of the second harmonic frequencies are substantially equal to the second transceiver carrier frequency; and

maintaining the second clock frequency for operating the at least one circuit as long as the passband uses the second transceiver carrier frequency.

26. (previously presented) The method of claim 25, wherein the first operation mode is one of a digital operation mode and an analog operation mode, and wherein the second operation mode is the other of the digital operation mode and the analog operation mode.

27. (previously presented) A method for reducing effects of clock harmonics in a plurality of communication passbands corresponding to a plurality of operation modes in a wireless communications device, the method comprising:

generating a clock signal at a clock frequency for driving a processor circuit, the clock signal having a plurality of harmonics frequencies;

generating a transceiver carrier signal in a transceiver for a first operation mode of the plurality of operation modes, the transceiver carrier signal at a carrier frequency for a first communication passband of the plurality of communication passbands for the first operation mode, wherein the carrier frequency is not substantially equal to any harmonic frequency of the plurality of harmonic frequencies;

changing the carrier frequency to a second carrier frequency for a second communication passband for a second operation mode of the plurality of operation modes, wherein the second carrier frequency is substantially equal to a harmonic frequency of the plurality of harmonic frequencies;

changing the clock frequency to a new clock frequency having a plurality of new harmonic frequencies, wherein the plurality of new harmonic frequencies are not substantially equal to the second carrier frequency; and

maintaining the new clock frequency for driving the processor circuit as long as the second carrier frequency is utilized.

28. (previously presented) The method of claim 27, wherein the plurality of operation modes comprise:

advanced mobile phone service (AMPS);

personal communication services (PCS);

global system for mobile communications (GSM);

code division multiple access (CDMA); and

wide-band code division multiple access (W-CDMA).

29. (previously presented) The method of claim 27, wherein the second operation mode is advanced mobile phone service (AMPS) with the second carrier frequency of approximately 900 megahertz, wherein the clock frequency is 19.2 megahertz having an interfering harmonic frequency of approximately 900 megahertz, and wherein the new clock frequency does not have the interfering harmonic frequency.

30. (previously presented) A system for reducing effects of spurious frequencies in a wireless communications device, the system comprising:

a microprocessor having a reference frequency input, a clock selection output, and a command selection output, the microprocessor for selecting operation modes for operating the wireless communications device in one of a digital mode and an analog mode, and for outputting the selected operation mode on the command selection output;

a clock having a clock output connected to the reference frequency input of the microprocessor, and an input connected to the clock selection output of the microprocessor, the clock outputting a first frequency clock corresponding to a first operation mode of the operation modes, the first frequency clock producing a first set of harmonic frequencies;

a transceiver for transceiving a first communication passband of a plurality of selectable communication passbands corresponding to the first operation mode, the transceiver then transceiving a second communication passband of the plurality of selectable communication passbands in response to a second operation mode received at a transciever input connected to the command selection output of the microprocessor, the first set of harmonic frequencies interfering with the second communication passband;

wherein the microprocessor selects a second frequency clock having a second set of harmonic frequencies that do not interfere with the second communication passband; and

wherein the second frequency clock is maintained on the reference frequency input as long as the second communication passband is selected.

31. (previously presented) The system of claim 30 wherein the microprocessor is one of a programmable logic device and a gate array.

32. (previously presented) The system of claim 30, wherein each selectable passband of the plurality of selectable communication passbands is associated with at least one operating mode of a plurality of operating modes comprising:

advanced mobile phone service (AMPS),

personal communication services (PCS),

global system for mobile communications (GSM),

code division multiple access (CDMA), and

wire-band CDMA (W-CDMA).

33. (previously presented) The system of claim 30, wherein the second operation mode is AMPS having the second communication passband with a center frequency of approximately 900 megahertz, wherein the first frequency clock is 19.2 megahertz having an interfering harmonic frequency of the first set of harmonic frequencies of approximately 900 megahertz, and wherein the second frequency clock does not have the interfering harmonic frequency.

34. (previously presented) A method for reducing effects of spurious frequencies in a wireless communications device, the method comprising the steps of:

operating a transceiver in a first mode of operation at a first passband frequency range of a plurality of selectable passband frequency ranges;

operating a logic device at a first clock frequency of a plurality of clock frequencies;

operating a transceiver in a second mode of operation at a second passband frequency range of a plurality of selectable passband frequency ranges such that the first clock frequency produces spurious frequencies in the second passband;

selecting a second clock frequency of the plurality of clock frequencies that produces no substantial spurious frequencies in the second passband frequency range;

operating the logic device at the selected second clock frequency; and

maintaining operation of the logic device with the selected second clock frequency during the operation of the transceiver in the second mode of operation.

35. (previously presented) The method of claim 34 wherein the logic device is a programmable logic device.

36. (previously presented) The method of claim 34 wherein the logic device is a gate array.

37. (previously presented) A wireless communications device comprising:

a transceiver operating in a CDMA mode having a first passband frequency range;

a clock operating at a first clock frequency of at least two clock frequencies, the first clock frequency producing no spurious signals in the first passband frequency range;

a processor operating at the first clock frequency, the processor comprising:

mode selection means for selecting an AMPS mode having a second passband frequency range;

processing means for determining a second clock frequency that produces no substantial spurious signals in the second passband frequency range, and;

clock control means for adjusting the clock to the second clock frequency, the clock control means maintaining the clock at the second clock frequency as long as the transceiver continues to operate in the AMPS mode; and,

an antenna connected to the transceiver.

38. (previously presented) A wireless communications device comprising:

a transceiver utilizing a carrier frequency for sending and receiving electromagnetic signals in an analog mode of operation;

a clock for generating a clock signal at a first frequency, the clock signal having a plurality of harmonics at a first plurality of harmonic frequencies;

a processor comprising:

carrier frequency control means for changing the carrier frequency to a second carrier frequency corresponding to a digital mode of operation, wherein the second carrier frequency is substantially equal to one harmonic frequency of the first plurality of harmonic frequencies; and

clock control means for changing the first frequency to a second frequency having

the plurality of harmonics at a second plurality of harmonic frequencies, wherein the second plurality of harmonic frequencies are not substantially equal to the second carrier frequency, the clock control means maintaining the second frequency until the carrier frequency control means changes the second carrier frequency to correspond to a new mode of operation; and

an antenna coupled to the transceiver.

39. (previously presented) A communication device for reducing effects of clock harmonic frequencies in a plurality of passband frequency ranges corresponding to a plurality of operational modes, the communication device comprising:

a transceiver clock circuit for generating a first passband frequency and a second passband frequency of the plurality of passband frequencies, the first passband frequency corresponding to a first operational mode and the second passband frequency corresponding to a second operational mode of the plurality of operational modes;

a transceiver connected to the transceiver clock circuit and operating in the first passband frequency range;

a processor clock circuit for generating a first operating frequency of a plurality of operating frequencies, the processor clock circuit outputting the first operating frequency on a clock output; and

a processor comprising:

a processor clock input connected to the clock output, the processor executing instruction sets utilizing any of the plurality of operating frequencies;

an operational mode selection output connected to the transceiver clock circuit for selecting the second operational mode of the plurality of operational modes;

a clock selection output connected to the processor clock circuit; and

processing means for determining whether the first operating frequency produces interfering harmonic frequencies that interfere with the second passband frequency, for outputting a clock selection on the clock selection output for selecting a non-interfering operating frequency of the plurality of

operating frequencies, for maintaining the selection of the non-interfering operating frequency on the clock selection output as long as the second operational mode remains selected.

40. (previously presented) The system of claim 39, wherein the second operational mode is AMPS having the second passband frequency of approximately 900 megahertz, wherein the first operational mode is CDMA having the first operating frequency of 19.2 megahertz with an interfering harmonic frequency of the interfering harmonic frequencies of approximately 900 megahertz, and wherein the non-interfering operating frequency does not have the interfering harmonic frequency.